WHAT IS CLAIMED IS:

1. A serial interface for use in a programmable logic device, said serial interface comprising:

a first number of physical medium attachment modules, at least a portion of said first number of said physical medium attachment modules supporting a first maximum physical medium attachment data rate; and

a second number of physical coding sublayer modules, each of said physical coding sublayer modules supporting a predetermined maximum physical coding sublayer data rate lower than said first maximum physical medium attachment data rate; wherein:

a respective plurality of said physical coding sublayer modules is connected to each of said physical medium attachment modules that supports said first maximum physical medium attachment data rate; whereby:

each said plurality of said physical coding sublayer modules supports each said physical medium attachment module at a data rate exceeding said predetermined maximum physical coding sublayer data rate up to said first maximum physical medium attachment data rate.

2. The serial interface of claim 1 wherein:

said interface is arranged as a plurality of channels, each of said channels including one of said physical coding sublayer modules and having a location for one of said physical medium attachment modules;

each respective plurality of physical coding sublayer modules includes physical coding sublayer modules from a respective group of multiple channels;

at least one channel in each said respective group of multiple channels includes a physical medium attachment module in said location; and

each respective plurality of physical coding sublayer modules is connected to a physical medium attachment module in one channel of its respective group of multiple channels.

3. The serial interface of claim 2 wherein:

at least one channel in at least one of said respective groups of multiple channels includes in said location a physical medium attachment module that supports a second maximum physical medium attachment data rate lower than said first maximum physical medium attachment data rate; and

said serial interface further comprises a selector for selectably connecting the physical coding sublayer module in said at least one channel to one of (a) said physical medium attachment module that supports said first maximum physical medium attachment data rate, and (b) said physical medium attachment module that supports said second maximum physical medium attachment data rate; whereby:

said at least one of said respective groups of multiple channels is selectably operable as one of (a) one channel at said first maximum physical medium attachment data rate, and (b) a plurality of channels at said second maximum physical medium attachment data rate.

4. The serial interface of claim 3 wherein said selector is controllable by user programming of said programmable logic device.

5. The serial interface of claim 3 wherein said selector is controllable by logic in said programmable logic device.

6. The serial interface of claim 3 wherein said selector is a multiplexer.

7. The serial interface of claim 3 wherein:

said physical medium attachment module that supports said first maximum physical medium attachment data rate also supports a first minimum physical medium attachment data rate; and

said physical medium attachment module that supports said second maximum physical medium attachment data rate also supports a second minimum physical medium attachment data rate lower than said first minimum physical medium attachment data rate; whereby:

any channel operated with one of said physical medium attachment modules that supports said first maximum physical medium attachment data rate is limited to operation at a rate above said first minimum physical medium attachment data rate.

8. The serial interface of claim 3 further comprising:

central logic, said central logic including:

a first clock source for generating a first clock signal at said first maximum physical medium attachment data rate for use as a transmit clock by said one channel operating at said first maximum physical medium attachment data rate.

9. The serial interface of claim 8 wherein said central logic further comprises a second clock source for generating a second clock signal at said second maximum physical medium attachment data rate for use as a transmit clock by any channel of said plurality of channels operating at said second maximum physical medium attachment data rate.

10. The serial interface of claim 2 further comprising:

central logic, said central logic including:

a clock source for generating a clock signal at said first maximum physical medium attachment

data rate for use as a transmit clock by said one channel operating at said first maximum physical medium attachment data rate.

11. A programmable logic device comprising the serial interface of claim 1.

12. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 11 coupled to the processing circuitry and the memory.

13. A printed circuit board on which is mounted a programmable logic device as defined in claim 11.

14. The printed circuit board defined in claim 13 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

15. The printed circuit board defined in claim 14 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

16. An integrated circuit device comprising the serial interface of claim 1.

17. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 16 coupled to the processing circuitry and the memory.

18. A printed circuit board on which is mounted an integrated circuit device as defined in claim 16.

19. The printed circuit board defined in claim 18 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

20. The printed circuit board defined in claim 19 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

21. A serial interface for use in a programmable logic device, said serial interface comprising:

a plurality of groups of two channels, each channel comprising a physical coding sublayer module and a physical medium attachment module; wherein, in each of said groups:

the physical medium attachment module in a first one said channels supports a first maximum physical medium attachment data rate;

the physical medium attachment module in a second one of said channels supports a second maximum physical medium attachment data rate lower than said first physical medium attachment data rate; and

each of said physical coding sublayer modules supports a predetermined maximum physical coding sublayer data rate lower than said first maximum physical medium attachment data rate; each of said groups further comprising:

a selector for selectably connecting the physical coding sublayer module in said second one of said channels to one of (a) said physical medium attachment module in said first one of said channels that supports a first maximum physical medium attachment data rate, and

(b) said physical medium attachment module in said second one of said channels that supports said second maximum physical medium attachment data rate; whereby:

each of said groups is selectably operable as one of (a) one channel at said first maximum physical medium attachment data rate, and (b) two channels at said second maximum physical medium attachment data rate.

22. The serial interface of claim 21 wherein said selector is controllable by user programming of said programmable logic device.

23. The serial interface of claim 21 wherein said selector is controllable by logic in said programmable logic device.

24. The serial interface of claim 21 wherein said selector is a multiplexer.

25. The serial interface of claim 21 wherein:

said physical medium attachment module that supports said first maximum physical medium attachment data rate also supports a first minimum physical medium attachment data rate; and

said physical medium attachment module that supports said second maximum physical medium attachment data rate also supports a second minimum physical medium attachment data rate lower than said first minimum physical medium attachment data rate; whereby:

any channel operated with one of said physical medium attachment modules that supports said first maximum physical medium attachment data rate is limited to operation at a rate above said first minimum physical medium attachment data rate.

26. The serial interface of claim 21 further comprising:

central logic, said central logic including:

a first clock source for generating a first clock signal at said first maximum physical medium attachment data rate for use as a transmit clock by said one channel operating at said first maximum physical medium attachment data rate.

27. The serial interface of claim 26 wherein said central logic further comprises a second clock source for generating a second clock signal at said second maximum physical medium attachment data rate for use as a transmit clock by any channel in any said group of two channels operating at said second maximum physical medium attachment data rate.

28. The serial interface of claim 21 comprising exactly two of said groups of two channels.

29. A programmable logic device comprising the serial interface of claim 11.

30. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 29 coupled to the processing circuitry and the memory.

31. A printed circuit board on which is mounted a programmable logic device as defined in claim 29.

32. The printed circuit board defined in claim 31 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

33. The printed circuit board defined in claim 32 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

34. An integrated circuit device comprising the serial interface of claim 11.

35. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 34 coupled to the processing circuitry and the memory.

36. A printed circuit board on which is mounted an integrated circuit device as defined in claim 34.

37. The printed circuit board defined in claim 36 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

38. The printed circuit board defined in claim 37 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.